# Atmel U6815BM

## Dual Hex DMOS Output Driver with Serial Input Control

**DATASHEET**

## Features

- Six high-side and six low-side drivers
- Outputs freely configurable as switch, half bridge, or H-bridge
- Capable to switch all kinds of loads such as DC motors, bulbs, resistors, capacitors and inductors
- 0.6A continuous current per switch
- Low-side: $R_{DSon}$ < 1.5Ω versus total temperature range
- High-side: $R_{DSon}$ < 2.0Ω versus total temperature range
- Very low quiescent current $I_S$ < 20µA in Standby Mode
- Outputs short-circuit protected
- Overtemperature prewarning and protection
- Under- and overvoltage protection
- Various diagnosis functions such as shorted output, open load, overtemperature and power supply fail
- Serial data interface
- Daisy chaining possible
- SO28 power package

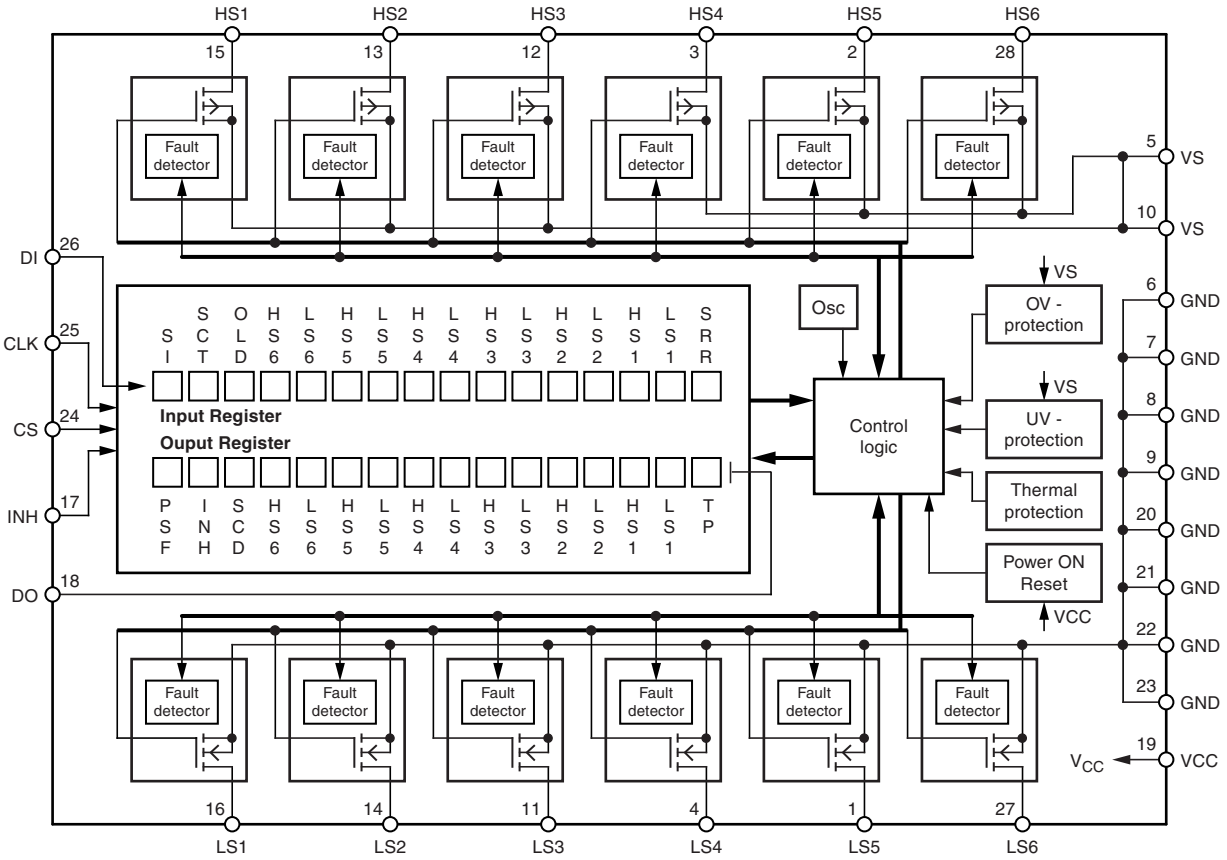
## Description

The Atmel® U6815BM is a fully protected driver interface designed in 0.8-µm BCDMOS technology. It is used to control up to 12 different loads by a microcontroller in automotive and industrial applications.

Each of the 6 high-side and 6 low-side drivers is capable of driving currents up to 600mA. The drivers are freely configurable and can be controlled separately from a standard serial data interface. Therefore, all kinds of loads such as bulbs, resistors, capacitors, and inductors can be combined. The IC design especially supports the applications of H-bridges to drive DC motors.

Protection is guaranteed for short-circuit conditions, overtemperature, under- and overvoltage. Various diagnostic functions and a very low quiescent current in standby mode enable a wide range of applications. The U6815BM has automotive qualification for conducted interferences, EMC protection, and 2-kV ESD protection.

**Figure 1. Block Diagram**



# 1. Pin Configuration

**Figure 1-1. Pinning SO28**

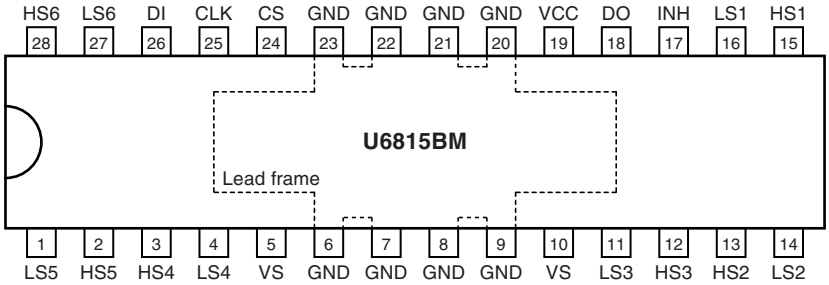



**Table 1-1. Pin Description**

| Pin | Symbol | Function |
|---|---|---|
| 1 | LS5 | Low-side driver output 5, power-MOS open drain with internal reverse diode, overvoltage protection by active zenering, short-circuit protection, diagnosis for short and open load |
| 2 | HS5 | High-side driver output 5, power-MOS open drain with internal reverse diode, overvoltage protection by active zenering, short-circuit protection, diagnosis for short and open load |
| 3 | HS4 | High-side driver output 4 (see pin 2) |
| 4 | LS4 | Low-side driver output 4 (see pin 1) |
| 5 | VS | Power supply output stages HS4, HS5, HS6, internal supply; external connection to pin 10 necessary |
| 6, 7, 8, 9 | GND | Ground, reference potential, internal connection to pin 20 to 23, cooling tab |
| 10 | VS | Power supply output stages HS1, HS2 and HS3 |
| 11 | LS3 | Low-side driver output 3 (see pin 1) |
| 12 | HS3 | High-side driver output 3 (see pin 2) |
| 13 | HS2 | High-side driver output 2 (see pin 2) |
| 14 | LS2 | Low-side driver output 2 (see pin 1) |
| 15 | HS1 | High-side driver output 1 (see pin 2) |
| 16 | LS1 | Low-side driver output 1 (see pin 1) |
| 17 | INH | Inhibit input, 5-V logic input with internal pull down, low = standby, high = normal operating |
| 18 | DO | Serial data output, 5-V CMOS logic level tristate output for output (status) register data, sends 16-bit status information to the microcontroller (LSB is transferred first). Output will remain tristated unless device is selected by CS = low, therefore, several ICs can operate on one data output line only. |
| 19 | VCC | Logic supply voltage (5V) |
| 20, 21, 22, 23 | GND | Ground (see pins 6 to 9) |
| 24 | CS | Chip select input, 5-V CMOS logic level input with internal pull-up, low = serial communication is enabled, high = disabled |
| 25 | CLK | Serial clock input, 5-V CMOS logic level input with internal pull-down, controls serial data input interface and internal shift register ($f_{max}$ = 2MHz) |
| 26 | DI | Serial data input, 5-V CMOS logic level input with internal pull-down, receives serial data from the control device, DI expects a 16-bit control word with LSB being transferred first |
| 27 | LS6 | Low-side driver output 6 (see pin 1) |
| 28 | HS6 | High-side driver output 6 (see pin 2) |

# 2. Functional Description

## 2.1 Serial Interface

Data transfer starts with the falling edge of the CS signal. Data must appear at DI synchronized to CLK and is accepted on the falling edge of the CLK signal. LSB (bit 0, SRR) must be transferred first. Execution of new input data is enabled on the rising edge of the CS signal. When CS is high, Pin DO is in tristate condition. This output is enabled on the falling edge of CS. Output data will change their state with the rising edge of CLK and stay stable until the next rising edge of CLK appears. LSB (bit 0, TP) is transferred first.

**Figure 2-1. Data Transfer**

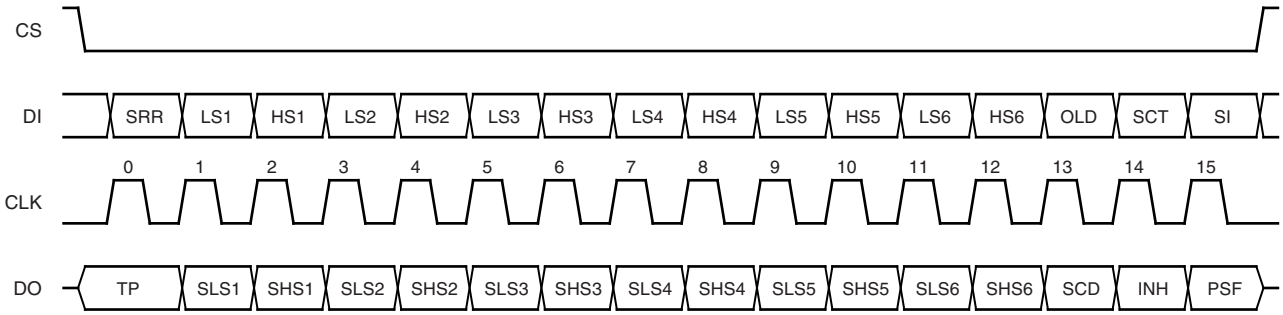



**Table 2-1. Input Data Protocol**

| Bit | Input Register | Function |
|---|---|---|
| 0 | SRR | Status register reset (high = reset; the bits PSF, SCD and overtemperature shutdown in the output data register are set to low) |
| 1 | LS1 | Controls output LS1 (high = switch output LS1 on) |
| 2 | HS1 | Controls output HS1 (high = switch output HS1 on) |
| 3 | LS2 | See LS1 |
| 4 | HS2 | See HS1 |
| 5 | LS3 | See LS1 |
| 6 | HS3 | See HS1 |
| 7 | LS4 | See LS1 |
| 8 | HS4 | See HS1 |
| 9 | LS5 | See LS1 |
| 10 | HS5 | See HS1 |
| 11 | LS6 | See LS1 |
| 12 | HS6 | See HS1 |
| 13 | OLD | Open-load detection (low = on) |
| 14 | SCT | Programmable time delay for short circuit and overvoltage shutdown (short-circuit shutdown delay high/low = 100 ms/12.5 ms, overvoltage shutdown delay high/low = 15ms/3.5ms |
| 15 | SI | Software inhibit; low = standby, high = normal operation (data transfer is not affected by standby function because the digital part is still powered) |

After power-on reset, the input register has the following status:

| Bit 15 (SI) | Bit 14 (SCT) | Bit 13 (OLD) | Bit 12 (HS6) | Bit 11 (LS6) | Bit 10 (HS5) | Bit 9 (LS5) | Bit 8 (HS4) | Bit 7 (LS4) | Bit 6 (HS3) | Bit 5 (LS3) | Bit 4 (HS2) | Bit 3 (LS2) | Bit 2 (HS1) | Bit 1 (LS1) | Bit 0 (SRR) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H | H | H | L | L | L | L | L | L | L | L | L | L | L | L | L |

**Table 2-2. Output Data Protocol**

| Bit | Output (Status) Register | Function |
|---|---|---|
| 0 | TP | Temperature prewarning: high = warning (overtemperature shut down)(1) |
| 1 | Status LS1 | Normal operation: high = output is on, low = output is off<br>Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off) |
| 2 | Status HS1 | Normal operation: high = output is on, low = output is off<br>Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off) |
| 3 | Status LS2 | Description see LS1 |
| 4 | Status HS2 | Description see HS1 |
| 5 | Status LS3 | Description see LS1 |
| 6 | Status HS3 | Description see HS1 |
| 7 | Status LS4 | Description see LS1 |
| 8 | Status HS4 | Description see HS1 |
| 9 | Status LS5 | Description see LS1 |
| 10 | Status HS5 | Description see HS1 |
| 11 | Status LS6 | Description see LS1 |
| 12 | Status HS6 | Description see HS1 |
| 13 | SCD | Short circuit detected: set high, when at least one output is switched off by a short-circuit condition |
| 14 | INH | Inhibit: this bit is controlled by software (bit SI in input register) and hardware inhibit (pin 17). High = standby, low = normal operation |
| 15 | PSF | Power supply fail: over- or undervoltage at pin VS detected |

Note: 1. Bit 0 to 15 = high: overtemperature shutdown

# 3. Power Supply Fail

In the event of over or undervoltage at pin VS, an internal timer is started. When the overvoltage delay time ($t_{dOV}$) programmed by the SCT Bit or the undervoltage delay time ($t_{dUV}$) is reached, the power-supply fail bit (PSF) in the output register is set and all outputs are disabled. When normal voltage is present again, the outputs are immediately enabled. The PSF bit remains high until it is reset by the SRR bit in the input register.

# 4. Open-load Detection

If the open-load detection bit (OLD) is set to low, a pull-up current for each high-side switch and a pull-down current for each low-side switch is turned on (open-load detection current $I_{HS1-6}$, $I_{LS1-6}$). If $V_{VS} - V_{HS1-6}$ or $V_{LS1-6}$ is lower than the open-load detection threshold (open-load condition), the corresponding bit of the output in the output register is set to high. Switching on an output stage with OLD bit set to low disables the open-load function for this output.

# 5. Overtemperature Protection

If the junction temperature exceeds the thermal prewarning threshold, $T_{jPW\ set}$, the temperature prewarning bit (TP) in the output register is set. When temperature falls below the thermal prewarning threshold $T_{jPW\ reset}$, the bit TP is reset. The TP bit can be read without transferring a complete 16-bit data word: with CS = high to low, the state of TP appears at Pin DO. After the microcontroller has read this information, CS is set high and the data transfer is interrupted without affecting the state of input and output registers.

If the junction temperature exceeds the thermal shutdown threshold $T_{j\ switch\ off}$, the outputs are disabled and all bits in the output register are set high. The outputs can be enabled again when the temperature falls below the thermal shutdown threshold, $T_{j\ switch\ on}$, and when a high has been written to the SRR bit in the input register. Thermal prewarning and shutdown threshold have hysteresis.

# 6. Short-circuit Protection

The output currents are limited by a current regulator. Current limitation takes place when the over-current limitation and shutdown threshold ($I_{HS1-6}$, $I_{LS1-6}$) are reached. Simultaneously, an internal timer is started. The shorted output is disabled during a permanent short when the delay time ($t_{dSd}$) programmed by the Short-Circuit Timer (SCT) bit is reached. Additionally, the Short-Circuit Detection (SCD) bit is set. If the temperature prewarning bit TP in the output register is set during a short, the shorted output is disabled immediately and SCD bit is set. By writing a high to the SRR bit in the input register, the SCD bit is reset and the disabled outputs are enabled.

## 6.1 Inhibit

There are two ways to disable the Atmel® U6815BM:

1. Set bit SI in the input register to zero
2. Switch Pin 17 (INH) to 0V

In both cases, all output stages are turned off but the serial interface stays active. The output stages can be activated again by bit SI = 1 or by pin 17 (INH) switched back to 5V.

## 7. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All values refer to GND pins.

| Parameters | Pins | Symbol | Value | Unit |
|---|---|---|---|---|
| Supply voltage | 5, 10 | $V_{VS}$ | –0.3 to +40 | V |
| Supply voltage, t < 0.5s; $I_S$ > –2A | 5, 10 | $V_{VS}$ | –1 | V |
| Supply voltage difference | $\|V_{S_Pin5} – V_{S_Pin10}\|$ | $\Delta V_{VS}$ | 150 | mV |
| Supply current | 5, 10 | $I_{VS}$ | 1.4 | A |
| Supply current, t < 200ms | 5, 10 | $I_{VS}$ | 2.6 | A |
| Logic supply voltage | 19 | $V_{VCC}$ | –0.3 to +7 | V |
| Input voltage | 17 | $V_{INH}$ | –0.3 to +17 | V |
| Logic input voltage | 24 to 26 | $V_{DI}$, $V_{CLK}$, $V_{CS}$ | –0.3 to $V_{VCC}$ + 0.3 | V |
| Logic output voltage | 18 | $V_{DO}$ | –0.3 to $V_{VCC}$ + 0.3 | V |
| Input current | 17, 24 to 26 | $I_{INH}$, $I_{DI}$, $I_{CLK}$, $I_{CS}$ | –10 to +10 | mA |
| Output current | 18 | $I_{DO}$ | –10 to +10 | mA |
| Output current | 1 to 4, 11 to 16 | $I_{LS1\ to}$ $I_{LS6}$ | Internally limited (see output specification) | mA |
| | 27, 28 | $I_{HS1\ to}$ $I_{HS6}$ | | mA |
| Output voltage | 2, 3, 12, 13, 15, 28 | HS1 to HS6 | –0.3 to +40 | V |
| | 1, 4, 11, 14, 16, 27 | LS1 to LS6 | | |
| Reverse conducting current ($t_{pulse}$ = 150µs) | 2, 3, 12, 13, 15, 28 towards 5, 10 | $I_{HS1\ to}$ $I_{HS6}$ | 17 | A |
| Junction temperature range | | $T_j$ | –40 to +150 | °C |
| Storage temperature range | | $T_{stg}$ | –55 to +150 | °C |

## 8. Thermal Resistance

All values refer to GND pins

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Junction - pin, measured to GND, Pins 6 to 9 and 20 to 23 | $R_{thJP}$ | 25 | K/W |
| Junction ambient | $R_{thJA}$ | 65 | K/W |

## 9. Operating Range

All values refer to GND pins

| Parameters | Pins | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | 5, 10 | $V_{VS}$ | $V_{UV}$(1) | | 40(2) | V |
| Logic supply voltage | 19 | $V_{VCC}$ | 4.5 | 5 | 5.5 | V |
| Logic input voltage | 17, 24 to 26 | $V_{INH}$, $V_{DI}$, $V_{CLK}$, $V_{CS}$ | –0.3 | | $V_{VCC}$ | V |
| Serial interface clock frequency | 25 | $f_{CLK}$ | | | 2 | MHz |
| Junction temperature | | $T_j$ | –40 | | +150 | °C |

Notes: 1. Threshold for undervoltage detection

2. Output disabled for $V_{VS}$ > $V_{OV}$ (threshold for overvoltage detection)

## 10. Noise and Surge Immunity

| Parameters | Test Conditions | Value |
|---|---|---|
| Conducted interferences | ISO 7637-1 | level 4(1) |
| Interference suppression | VDE 0879 Part 2 | level 5 |
| ESD (human body model) | MIL-STD-883D Method 3015.7 | 2kV |
| ESD (machine model) | EOS/ESD - S 5.2 | 150V |

Note: 1. Test pulse 5: $V_{Smax}$ = 40V

## 11. Electrical Characteristics

7.5V < $V_{VS}$ < 40V; 4.5V < $V_{VCC}$ < 5.5V; INH = High; –40°C < Tj < 150°C; unless otherwise specified, all values refer to GND pins.

| Parameters | Test Conditions/Pins | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Current Consumption | | | | | | |
| Quiescent current ($V_S$) | $V_{VS}$ < 16V, INH or bit SI = low<br>Pins 5, 10 | $I_{VS}$ | | | 40 | µA |
| Quiescent current ($V_{CC}$) | 4.5V < $V_{VCC}$ < 5.5V,<br>INH or bit SI = low, pin 19 | $I_{VCC}$ | | | 20 | µA |
| Supply current ($V_S$)<br>normal operating | $V_{VS}$ < 16V, pins 5, 10<br>all output stages off | $I_{VS}$ | | 0.8 | 1.2 | mA |
| | All output stages on, no load | $I_{VS}$ | | | 10 | mA |
| Supply current ($V_{CC}$) | 4.5V < $V_{VCC}$ < 5.5V,<br>normal operating, pin 19 | $I_{VCC}$ | | | 150 | µA |
| Internal Oscillator Frequency | | | | | | |
| Frequency<br>(time-base for delay timers) | | $f_{OSC}$ | 19 | | 45 | kHz |
| Over- and Undervoltage Detection, Power-on Reset | | | | | | |
| Power-on reset threshold | Pin 19 | $V_{VCC}$ | 3.4 | 3.9 | 4.4 | V |
| Power-on reset delay time | After switching on $V_{VCC}$ | $t_{dPor}$ | 30 | 95 | 160 | µs |
| Undervoltage detection threshold | Pins 5, 10 | $V_{UV}$ | 5.5 | | 7.0 | V |
| Undervoltage detection hysteresis | Pins 5, 10 | $\Delta V_{UV}$ | | 0.4 | | V |
| Undervoltage detection delay | | $t_{dUV}$ | 7 | | 21 | ms |
| Overvoltage detection threshold | Pins 5, 10 | $V_{OV}$ | 18 | | 22.5 | V |
| Overvoltage detection hysteresis | Pins 5, 10 | $\Delta V_{OV}$ | | 1 | | V |
| Overvoltage detection delay | Input register, Bit 14 (SCT) = high | $t_{dOV}$ | 7 | | 21 | ms |
| Overvoltage detection delay | Input register, Bit 14 (SCT) = low | $t_{dOV}$ | 1.75 | | 5.25 | ms |
| Thermal Prewarning and Shutdown | | | | | | |
| Thermal prewarning, set | | $T_{jPWset}$ | 125 | 145 | 165 | °C |
| Thermal prewarning, reset | | $T_{jPWreset}$ | 105 | 125 | 145 | °C |
| Thermal prewarning hysteresis | | $\Delta T_{jPW}$ | | 20 | | K |
| Thermal shutdown, off | | $T_{j\ switch\ off}$ | 150 | 170 | 190 | °C |
| Thermal shutdown, on | | $T_{j\ switch\ on}$ | 130 | 150 | 170 | °C |
| Thermal shutdown hysteresis | | $\Delta T_{j\ switch\ off}$ | | 20 | | K |

Notes: 1. Only valid for version U6815BM-N.
2. Delay time between rising edge of CS after data transmission and switch-on output stages to 90% of final level.

## 11. Electrical Characteristics (Continued)

7.5V < $V_{VS}$ < 40V; 4.5V < $V_{VCC}$ < 5.5V; INH = High; –40°C < Tj < 150°C; unless otherwise specified, all values refer to GND pins.

| Parameters | Test Conditions/Pins | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Ratio thermal shutdown, off/thermal prewarning, set | | $T_{j\ switch\ off}$/ $T_{jPW\ set}$ | 1.05 | 1.17 | | |
| Ratio thermal shutdown, on/thermal prewarning, reset | | $T_{j\ switch\ on}$/ $T_{jPW\ reset}$ | 1.05 | 1.2 | | |
| Output Specification (LS1 to LS6, HS1 to HS6), 7.5V < $V_{VS}$ < $V_{OV}$ | | | | | | |
| On resistance, low | $I_{Out}$ = 600mA, Pins 1, 4, 11, 14, 16 and 27 | $R_{DS\ On\ L}$ | | | 1.5 | Ω |
| On resistance, high | $I_{Out}$ = –600mA, Pins 2, 3, 12, 13, 15 and 28 | $R_{DS\ On\ H}$ | | | 2.0 | Ω |
| Output clamping voltage | $I_{LS1–6}$ = 50mA, Pins 1, 4, 11, 14, 16, 27 | $V_{LS1–6}$ | 40 | | 60 | V |
| Output leakage current | $V_{LS1–6}$ = 40V, all output stages off, Pins 1, 4, 11, 14, 16 and 27 | $I_{LS1–6}$ | | | 10 | µA |
| | $V_{HS1–6}$ = 0V, all output stages off, Pins 2, 3, 12, 13, 15 and 28 | $I_{HS1–6}$ | –10 | | | µA |
| Inductive shutdown energy[1] | Pins 1-4, 11-16, 27 and 28 | $W_{outx}$ | | | 15 | mJ |
| Output voltage edge steepness | Pins 1-4, 11-16, 27 and 28 | $dV_{LS1–6}/dt$ $dV_{HS1–6}/dt$ | 50 | 200 | 400 | mV/µs |
| Overcurrent limitation and shutdown threshold | Pins 1, 4, 11, 14, 16 and 27 | $I_{LS1–6}$ | 650 | 950 | 1250 | mA |
| | Pins 2, 3, 12, 13,15 and 28 | $I_{HS1–6}$ | –1250 | –950 | –650 | mA |
| Overcurrent shutdown delay time | Input register, bit 14 (SCT) = high | $t_{dSd}$ | 70 | 100 | 140 | ms |
| | Input register, bit 14 (SCT) = low | $t_{dSd}$ | 8.75 | | 17.5 | ms |
| Open-load detection current | Input register, bit 13 (OLD) = low, output off, pins 1, 4, 11, 14, 16, 27 | $I_{LS1–6}$ | 60 | | 200 | µA |
| | Input register, bit 13 (OLD) = low, output off, pins 2, 3, 12, 13, 15, 28 | $I_{HS1–6}$ | –150 | | –30 | µA |
| Open-load detection current ratio | | $I_{LS1–6}$/ $I_{HS1–6}$ | 1.2 | | | |
| Open-load detection threshold | Input register, bit 13 (OLD) = low, output off, pins 1, 4, 11, 14, 16, 27 | $V_{LS1–6}$ | 0.6 | | 4 | V |
| | Input register, bit 13 (OLD) = low, output off, pins 2, 3, 12, 13, 15, 28 | $V_{VS–}$ $V_{HS1–6}$ | 0.6 | | 4 | V |
| Output switch on delay [2] | $R_{Load}$ = 1kΩ | $t_{don}$ | | | 0.5 | ms |
| | $R_{Load}$ = 1kΩ | $t_{doff}$ | | | 1 | ms |
| Inhibit Input | | | | | | |
| Input voltage low level threshold | Pin 17 | $V_{IL}$ | 0.3 × $V_{VCC}$ | | | V |
| Input voltage high level threshold | Pin 17 | $V_{IH}$ | | | 0.7× $V_{VCC}$ | V |
| Hysteresis of input voltage | Pin 17 | $\Delta V_I$ | 100 | | 700 | mV |
| Pull-down current | $V_{INH}$ = $V_{VCC}$, pin 17 | $I_{PD}$ | 10 | | 80 | µA |

Notes: 1. Only valid for version U6815BM-N.

2. Delay time between rising edge of CS after data transmission and switch-on output stages to 90% of final level.

## 11. Electrical Characteristics (Continued)

7.5V < $V_{VS}$ < 40V; 4.5V < $V_{VCC}$ < 5.5V; INH = High; –40°C < Tj < 150°C; unless otherwise specified, all values refer to GND pins.

| Parameters | Test Conditions/Pins | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Serial Interface - Logic Inputs (DI, CLK, CS) | | | | | | |
| Input voltage low level threshold | Pins 24 to 26 | $V_{IL}$ | 0.3 × $V_{VCC}$ | | | V |
| Input voltage high level threshold | Pins 24 to 26 | $V_{IH}$ | | | 0.7 × $V_{VCC}$ | V |
| Hysteresis of input voltage | Pins 24 to 26 | $\Delta V_I$ | 50 | | 500 | mV |
| Pull-down current, Pins DI and CLK | $V_{DI}$, $V_{CLK}$ = $V_{VCC}$, pins 25, 26 | $I_{PDSI}$ | 2 | | 50 | µA |
| Pull-up current Pin CS | $V_{CS}$= 0V, pin 24 | $I_{PUSI}$ | –50 | | –2 | µA |
| Serial Interface - Logic Output (DO) | | | | | | |
| Output voltage low level | $I_{OL}$ = 3 mA, pin 18 | $V_{DOL}$ | | | 0.5 | V |
| Output voltage high level | $I_{OL}$ = –2 mA, pin 18 | $V_{DOH}$ | $V_{VCC}$ – 1V | | | V |
| Leakage current (tristate) | $V_{CS}$ = $V_{VCC}$, 0V < $V_{DO}$ < $V_{VCC}$, pin 18 | $I_{DO}$ | –10 | | 10 | mA |

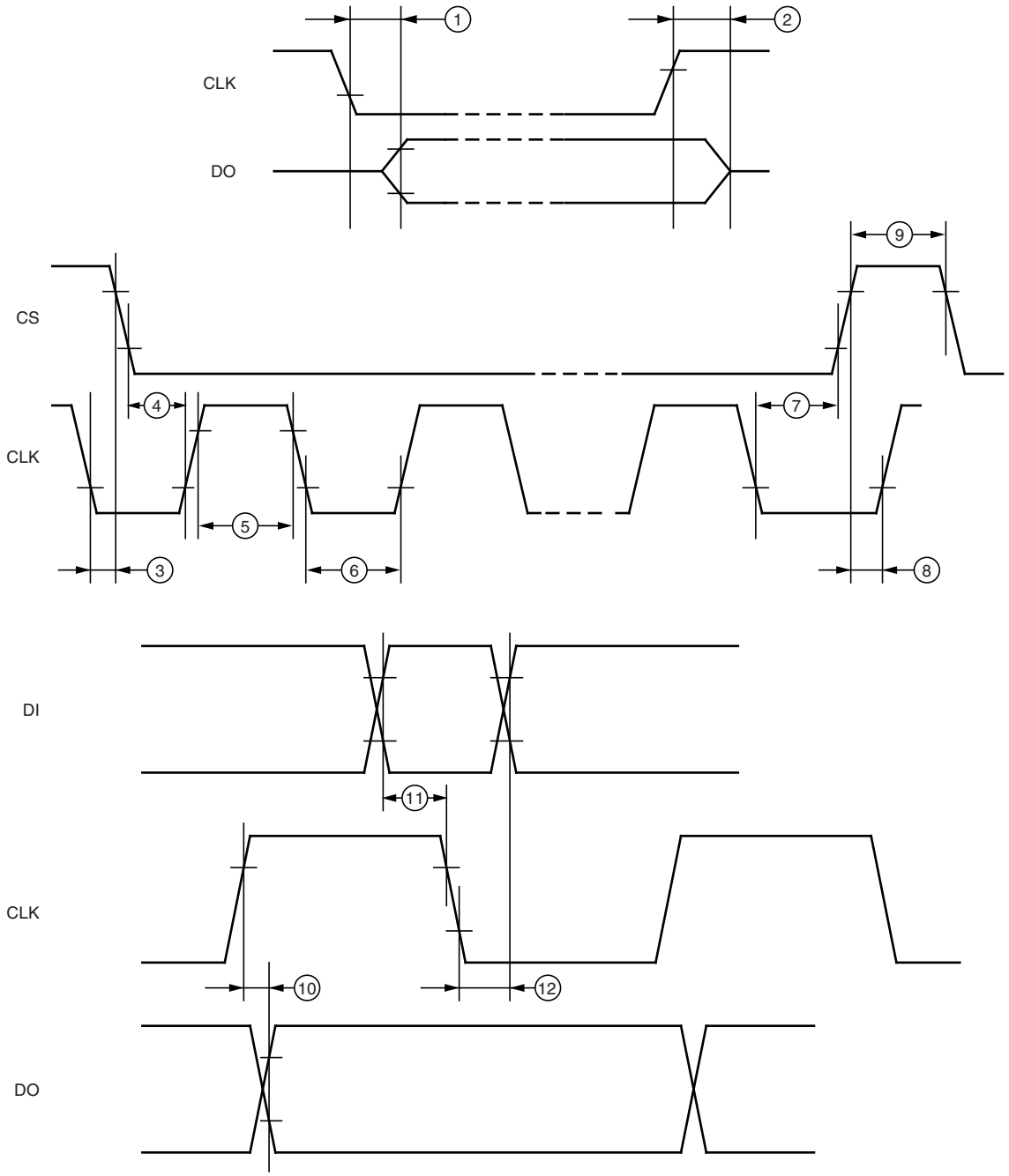
Notes: 1. Only valid for version U6815BM-N.
2. Delay time between rising edge of CS after data transmission and switch-on output stages to 90% of final level.

## 12. Serial Interface – Timing

| Parameters | Test Conditions | Timing Chart No.(1) | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| DO enable after CS falling edge | $C_{DO}$ = 100pF | 1 | $t_{ENDO}$ | | | 200 | ns |
| DO disable after CS rising edge | $C_{DO}$ = 100pF | 2 | $t_{DISDO}$ | | | 200 | ns |
| DO fall time | $C_{DO}$ = 100pF | – | $t_{DOf}$ | | | 100 | ns |
| DO rise time | $C_{DO}$ = 100pF | – | $t_{DOr}$ | | | 100 | ns |
| DO valid time | $C_{DO}$ = 100pF | 10 | $t_{DOVal}$ | | | 200 | ns |
| CS setup time | | 4 | $t_{CSSethl}$ | 225 | | | ns |
| CS setup time | $V_{DO}$ < 0.2 × $V_{VCC}$ | 8 | $t_{CSSetlh}$ | 225 | | | ns |
| CS high time | Input register, Bit 14 (SCT) = high | 9 | $t_{CSh}$ | 140 | | | ms |
| | Input register, Bit 14 (SCT) = low | 9 | $t_{CSh}$ | 17.5 | | | ms |
| CLK high time | | 5 | $t_{CLKh}$ | 225 | | | ns |
| CLK low time | | 6 | $t_{CLKl}$ | 225 | | | ns |
| CLK period time | | – | $t_{CLKp}$ | 500 | | | ns |
| CLK setup time | | 7 | $t_{CLKSethl}$ | 225 | | | ns |
| CLK setup time | | 3 | $t_{CLKSetlh}$ | 225 | | | ns |
| DI setup time | | 11 | $t_{DIset}$ | 40 | | | ns |
| DI hold time | | 12 | $t_{DIHold}$ | 40 | | | ns |

Note: 1. See Figure 12-1 on page 11

**Figure 12-1. Serial Interface Timing Diagram with Chart Numbers**

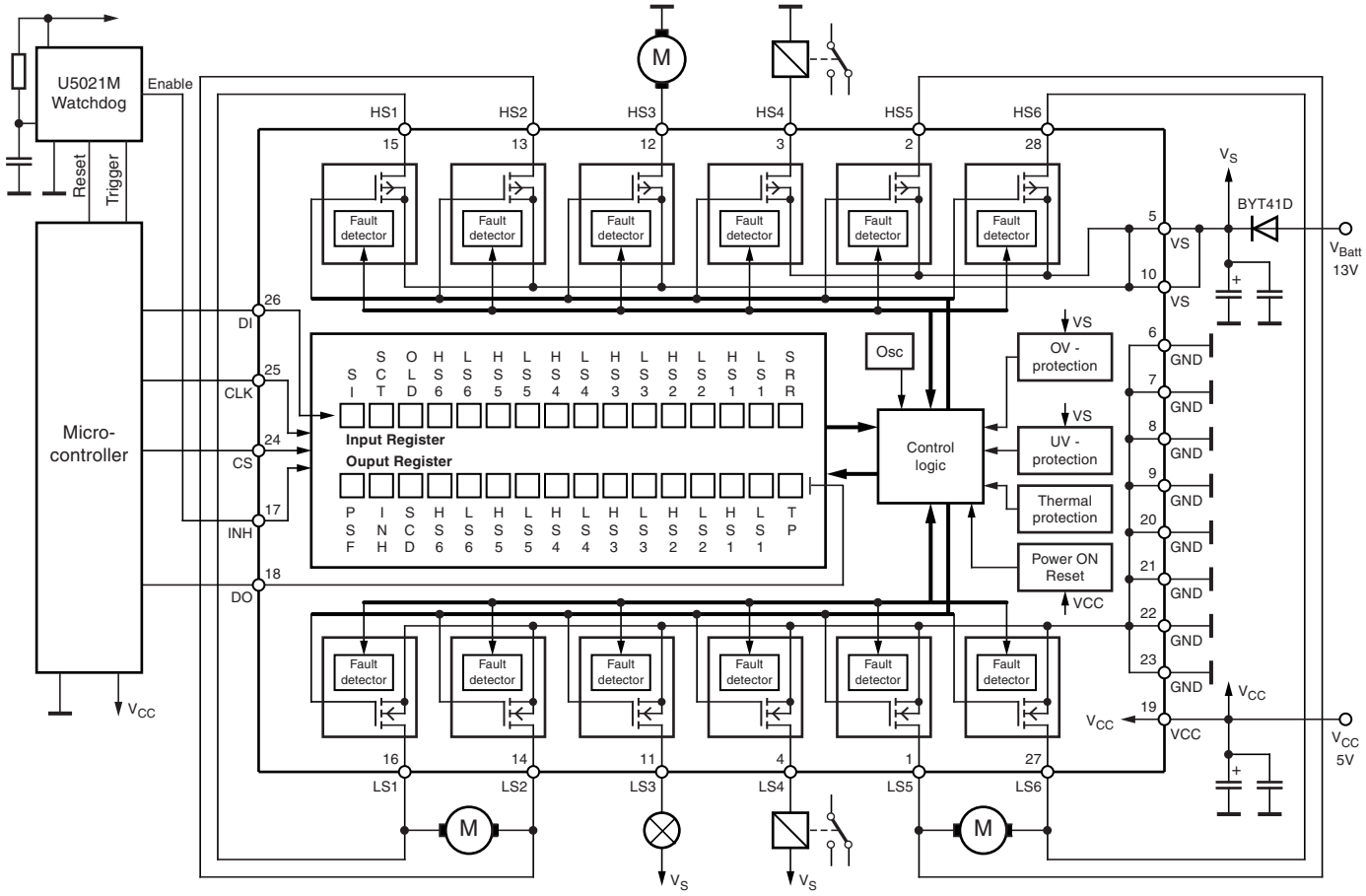



Inputs DI, CLK, CS: High level = 0.7 × $V_{CC}$, Low level = 0.3 × $V_{CC}$

Output DO: High level = 0.8 × $V_{CC}$, Low level = 0.2 × $V_{CC}$

For chart numbers, see Table "Serial Interface – Timing" on page 10.

**Figure 12-2. Application Circuit**




## 13. Application Notes

It is strongly recommended to connect the blocking capacitors at $V_{CC}$ and $V_S$ as close as possible to the power supply and GND pins.

Recommended value for capacitors at $V_S$:

Electrolytic capacitor C > 22µF in parallel with a ceramic capacitor C = 100nF. Value for electrolytic capacitor depends on external loads, conducted interferences, and reverse conducting current $I_{HSx}$ (see table Absolute Maximum Ratings).

Recommended value for capacitors at $V_{CC}$:

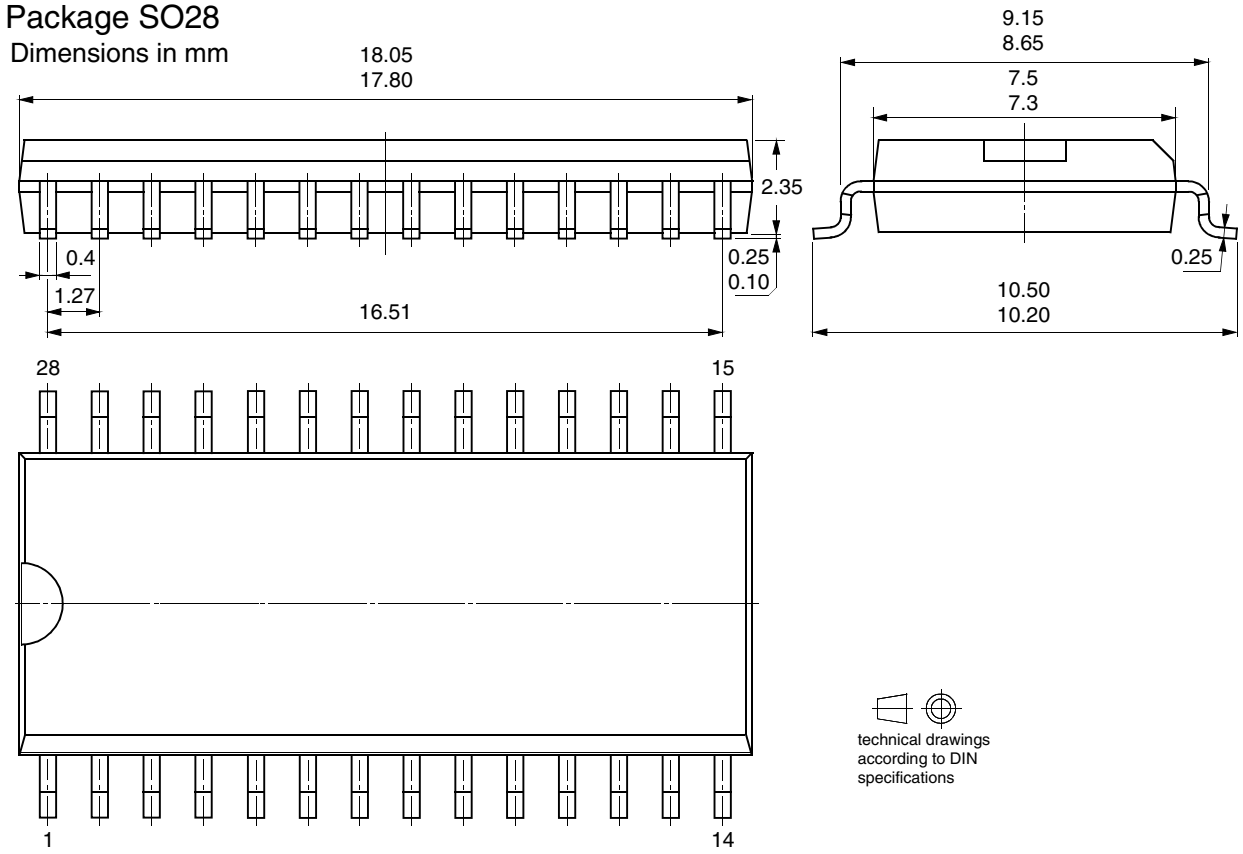
Electrolytic capacitor C > 10µF in parallel with a ceramic capacitor C = 100nF. To reduce thermal resistance, it is recommended to place cooling areas on the PCB as close as possible to the GND pins.

## 14. Ordering Information

| Extended Type Number | Package | Remarks |
|---|---|---|
| U6815BM-NFLY | SO28 | Tubed, Pb-free |

## 15. Package Information

**Figure 15-1. SO28**




## 16. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

| Revision No. | History |
|---|---|
| 4545E-AUTO-06/12 | • Section 14 “Ordering Information” on page 13 changed |
| 4545D-BCD-04/09 | • Put datasheet in a new template<br>• Absolute Maximum Ratings table changed |
| 4545C-BCD-09/05 | • Put datasheet in a new template<br>• Pb-free logo on page 1 added<br>• New heading rows on Table “Absolute Maximum Ratings” on page 7 added<br>• Table “Ordering Information” on page 13 changed |

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